

Appl. Math. Lett. Vol. 6, No. 3, pp. 33–36, 1993
 Printed in Great Britain. All rights reserved

0893-9659/93 \$6.00 + 0.00
 Copyright©1993 Pergamon Press Ltd

A SERIES OF IMPULSE FUNCTIONS AS A MODEL FOR RANDOM DETECTABILITY PROFILES

H. A. FARHAT

Department of Mathematics and Computer Science
 University of Nebraska, Omaha, NE 68182, U.S.A.

(Received and accepted February 1993)

Abstract—We model the detectability distribution as a series of impulse functions. The advantages of the presented work on previous related work is in the generality of the model and the simplicity of computing its parameters.

INTRODUCTION

In production testing of VLSI circuits, input patterns are applied to a manufactured chip; the chip's output is then compared to a known "good" response. A mismatch between the circuit output and a stored good response signals a physical failure. An important aspect of this, is to find the needed test set (input patterns). For small combinational circuits with small number of inputs, the test set can be exhaustive. That is, the entire input space can be used as a test set. However, since the size of the input space grows exponentially in the number of inputs, exhaustive testing is infeasible and costly for large circuits. As a result, one usually searches the input space for a subset of inputs that can be used as a test.

The test set generation problem of a VLSI circuit is to find this subset of the input space [1]. This problem has been known to be NP-Complete for sometime [2]. In generating such a test, one employs two algorithms: (a) a *deterministic* test generator [1], and (b) a *fault simulator* [3]. The deterministic test generation algorithm generates a test for a specific target fault. A fault simulation algorithm then finds all other modeled faults detected by the generated test. In terms of costs (CPU time, memory space requirements, etc.), the costs of fault simulation grow nonlinearly in the size of the fault population. In fact, these costs dominate the overall costs of test generation for sequential circuits and large combinational circuits. In [4], it was reported that for a sequential chip with 4856 faults, to generate a test sequence of 842 inputs, the total test generation time was 64062 seconds (17.795 hours of CPU time!). When fault simulation was carried on a sample of 1000 faults and the entire fault population, the computation time was 86585 and 462234 seconds, respectively.

Reducing the costs of fault simulation is the primary reason for this work and previous related work. To do this, we employ a relation between coverage and the detectability profile of a circuit (detection probability distribution). In [5], the detectability distribution was estimated as beta model. The beta model is a two parameter continuous model, however. Actual detectability distributions are discrete in nature and can be represented as a sequence of impulse functions (see Figure 1 for SN74181 4 bit ALU). Accordingly, we model the detectability profile as a series of impulse functions located at predetermined intervals. However, unlike previous work [6], we use sample coverage data to estimate the parameters for detectability. In addition, we use fault dropping in estimating the parameters (this will further reduce the costs of fault simulation).

DEFINITIONS

The *detection probability* of a modeled fault α is the probability of detecting α by a random input. A fault is called *redundant* if its detection probability is equal to zero. Because of the NP-complete nature of the deterministic test generator, one usually imposes a time limit on

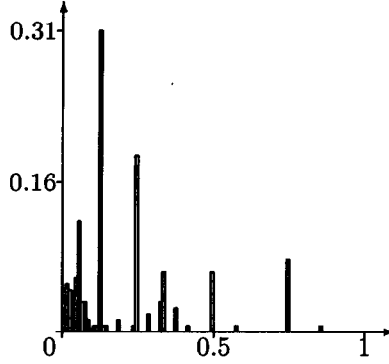


Figure 1. Detectability profile for SN74181.

the CPU computations of any implementation of a test generation algorithm. Target faults not detected within the specified time limit are classified as *aborted*. The *detection probability distribution* (*detectability profile*), $p(x)$, of a combinational circuit is the probability density function of detection probabilities of faults in the circuit. The *fault coverage*, y_n , of a set of vectors is the fraction of faults detected by the vectors.

THE DETECTABILITY AND COVERAGE RELATION

For detailed analysis, the interested reader is referred to [4]. Assume n random vectors are applied to a circuit with some known $p(x)$ distribution. The expected coverage, y_n , by the n vectors is, $y_n = 1 - \int_0^1 (1-x)^n p(x) dx = 1 - I(n)$. For deterministic coverage, each newly generated vector detects at least one new fault not detected by already generated tests. Accordingly, the deterministic coverage by n vectors, y_n , can be found as $y_n = 1 - I(n) + n/Y \left[1 + I(n) - \int_0^1 ((1-(1-x)^n)/nx) p(x) dx \right] \approx 1 - I(n) + n/Y$.

THE DETECTABILITY MODEL

In accordance with actual detectability profiles of a VLSI circuit, we model $p(x)$ as

$$p(x) = \sum_{i=0}^k \alpha_i \delta(x - x_i), \quad \text{and hence,} \quad (1)$$

$$y_n = (1 - \alpha_0) - \sum_{i=1}^k \alpha_i e^{[\ln(1-x_i)]n}. \quad (2)$$

Note that the random coverage distribution for this model is given in terms of the α parameters of detectability profile. The relation has an intuitive explanation. The $1 - \alpha_0$ term represents the maximum possible attainable random coverage (α_0 is the fraction of undetectable faults). The remaining term $(\sum_{i=1}^k \alpha_i e^{[\ln(1-x_i)]n})$ represents a sum of exponentially decaying functions; as n increases, this term approaches zero. Hence, the random coverage distribution assumes an exponential rise with asymptotic value of $1 - \alpha_0$.

The parameters of the detectability model can be estimated from *initial* coverage data on a sample of faults. The estimation provides two important results. First, a new method of estimating the detectability distribution from partial fault coverage data is given. Second, the detectability model can be used to predict fault coverage of tests not yet generated. The prediction of fault coverage can answer important testability questions about the circuit without the need to employ full test generation or fault simulation.

ESTIMATING DETECTABILITY

Assume $p(x)$ is modeled as $p(x) = \sum_{i=0}^9 \alpha_i \delta(x - 0.1i)$, where $\delta(x - x_0)$ is the Dirac delta function at x_0 , $\sum_{i=0}^9 \alpha_i = 1$, and $\alpha_i \geq 0$ for $i = 0, 1, \dots, 9$. That is, $p(x)$ is modeled as a series

of 10 impulse functions equally spaced on the interval $[0,1]$ with α_0 equal to the strength of the impulse function at zero. (Here, 10 equally spaced functions are chosen for simplicity; later it is shown that more impulse functions near zero are needed for this distribution to be effective.) Substituting $p(x)$ in the equation for random coverage one obtains

$$y_n = 1 - \sum_{i=0}^{i=9} \alpha_i (1 - 0.1i)^n. \quad (3)$$

Assume that the random coverage is known for at least the first 9 vectors. Denote the known coverage in increasing order as y_1, y_2, \dots, y_9 . From the above, we obtain the following system of linear equations

$$C = AX, \quad (4)$$

where

$$\begin{aligned} c_i &= 1 - y_i, & c_0 &= 1, \\ x_i &= \alpha_i, & \text{and} \\ a_{ij} &= (1 - 0.1j)^i, & i, j &= 0, 1, 2, \dots, 9. \end{aligned}$$

Equation (2) can be solved numerically by standard methods to obtain the values of $\alpha_0, \alpha_1, \dots, \alpha_9$. Unfortunately, the coverage y_i is a function of the type of vectors used (the coverage of the initial vectors, under 5 vectors, can vary by as much as 20%). This variance in coverage is removed, however, as the test generation process proceeds and large number of vectors are generated. That is, the coverage y_n is approximately constant for large n ($n > 20$). To take this fact into account, one can generate enough vectors and compute the coverage values of the generated vectors. The coverage data collected can then be used to predict the parameters of detectability using statistical methods such as the least squares fit method.

For high coverage estimation, the detectability distribution near zero is very significant. As a result, the detectability model should contain many impulse functions near zero. To take this into account and to remove singularities that may occur from including many impulse functions near zero, the detectability model selected is as follows.

Assume the coverage by the first N vectors is known ($N \gg 10$). Estimate the parameters in

$$p'(x) = \beta_0 \delta(x) + \beta_1 \delta\left(x - \frac{1}{N}\right) + \sum_{i=1}^k \alpha_i \delta(x - x_i) \quad (5)$$

using a statistical package such as "Minitab." From the above estimated parameters, form the detectability model

$$\begin{aligned} p(x) &= \frac{1}{k \cdot (k+1)} * \left[\sum_{i=1}^k \left((k-i)(\beta_0 - \beta'_0) + \beta_1 \cdot i \right) \delta\left(x - \frac{i}{k \cdot N}\right) \right] \\ &+ \beta'_0 \delta(x) + \sum_{i=1}^9 \alpha_i \delta(x - x_i), \end{aligned} \quad (6)$$

where β'_0 is the fraction of redundant and aborted faults, and k is the number of impulse functions in the interval $[0, 1/N]$. In the above equation, the strength of the impulse functions in the interval $[0, 1/N]$ was chosen as a linear combination of the strength of the estimated impulse functions at $1/N$ and zero (excluding redundant and aborted faults), respectively. The model distributes the contribution of the impulse functions in a linear fashion.

EXPERIMENTAL RESULTS

The proposed method of computing the parameters of $p(x)$ was carried on two of the largest ISCAS-89 circuits [7]: s35932, and s38584. A podem test generator [1] and a deductive fault simulator [3] were used in the initial test generation process. A random sample of 500 faults was chosen from the fault population of each circuit (39094 and 36303 faults for s35932 and

s38584, respectively). The number of tests generated to obtain 100% sample coverage (excluding redundant and hard-to-test faults) were 27 for the s35932 circuit and 80 for the s38584 circuit, respectively.

To compute the detectability parameters using the least squares method, the Minitab statistical package was used. Here, however, in computing the parameters, we used sample coverage data. That is, fault simulation with fault dropping was used. The fact that the coverage data on a sample of faults were used in the computations and that fault dropping was used in simulation makes this procedure computationally more efficient than earlier work. From the estimated parameters, the detectability profile of each of the circuits were computed using equation (5). From detectability profile, the *estimated* coverage distribution was computed.

To compare the estimated coverage data to actual coverage, tests were generated in a separate run for each of the two circuits. The tests generated employed full fault simulation on the entire fault population. The number of tests generated were 78 and 900 vectors for s35932 and s38584, respectively. Table 1 includes a comparison between the estimated coverage data for the other two circuits. From a test generation point of view, the estimates for high coverage are more significant than early coverage (the test engineer is usually more interested in the cumulative coverage of a set of vectors and not in the coverage of individual vectors). Thus, initial inaccuracies in the coverage data are not significant in the analysis.

Table 1.

Circuit s35932			Circuit s38584		
Vectors	Coverage Actual	Coverage Estimated	Vectors	Coverage Actual	Coverage Estimated
1	29.45	44.02	1	22.56	31.46
20	86.47	87.91	100	85.65	85.25
30	88.29	87.91	500	92.53	92.18
50	89.40	88.28	700	94.20	93.86
78	89.80	88.62	900	95.50	95.14

CONCLUSION

In this paper, a new method of computing the detection probability distribution and estimating the coverage distribution was presented. The advantages of this work on previous related work are:

- (1) in using a detectability model that closely resembles actual detectability profiles, and
- (2) in estimating detectability, we employ fault simulation on the sample with fault dropping.

REFERENCES

1. P. Goel, An implicit enumeration algorithm to generate tests for combinational logic circuits, *IEEE Trans. Computers* C-30, 215-222, March 1981; Also *Fault-Tol. Comp. Symp.* (FTCS010) Digest of Papers, Kyoto, Japan, October 1980, pp. 145-151.
2. O.H. Ibarra, S.K. Sahni, Polynomially complete fault detection problems, *IEEE. Trans. Comp.* C-24, 242-249 (1975).
3. D.B. Armstrong, A deductive method for simulating faults in logic circuits, *IEEE Trans. Computers* C-21, 464-471 (May 1972).
4. S.C. Seth, V.D. Agrawal and H.A. Farhat, A statistical theory of digital circuit testability, *IEEE Trans. Computers* 39 (4), 582-586 (April 1990).
5. H.A. Farhat, S.G. From, A beta testability model for estimating the testability and coverage distributions of a VLSI circuit, *IEEE Transactions on Computer-Aided Design* (to appear).
6. H.A. Farhat, M. Zand, H. Saiedian, Estimating testability and coverage distributions of a VLSI circuit from a mixture of discrete and continuous functions, Presented at the *ACM Symposium on Applied Computing*, Kansas City, (March 1-3, 1992).
7. F. Brglez, D. Bryan, and K. Kozminski, Combinational profiles of sequential benchmark circuits, In *Proc. Int. Symp. on Circuits and Systems*, Portland, OR, 1929-1934, (May 1989).